

FLASH MEMORY CELL STRUCTURE AND OPERATING METHOD THEREOF

Abstract

A flash memory cell structure has a substrate, a select gate, a first-type doped region, a shallow second-type doped region, a deep second-type doped region, and a doped source region. The substrate has a stacked gate. The select gate is formed on the substrate and adjacent to the stacked gate. The first-type ion formed region is doped in the substrate and adjacent to the select gate as a drain. The shallow second-type doped region is formed on one side of the first-type doped region below the stacked gate. The deep second-type doped region, which serves as a well, is formed underneath the first-type doped region with one side bordering on the shallow second-type doped region. The doped source region is formed on a side of the shallow second-type doped region as a source.